

# Performance Evaluation and Comparative Study of Double Gate SOI MOSFET and FinFET using Silvaco TCAD Tool

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**Abstract-** Transistor size is decreasing day by day, therefore it is difficult to overcome the problem of short channel effects. For preventing short channel effects, source/drain engineering, substrate engineering & gate engineering have been introduced. According to chronological growth of VLSI Design, there is need of non-conventional structure of MOSFET and researchers are getting shifted in search of other structure of transistor such as Silicon on Insulator MOSFET, Double Gate MOSFET and FinFET. In this paper, the semiconductor physics and basic electrical properties of Double Gate MOSFET and FinFET have been described. The performance evaluation and comparative study have been done by various performance parameters with the help of SILVACO TCAD tool. The study shows that Double Gate MOSFET and FinFET have better results than conventional MOSFET and are better option for reducing short channel effects.

**Keywords-** Short Channel effects, Double Gate MOSFET and FinFET

## I. INTRODUCTION

With the continuous scaling of MOSFET, the transistor size is moving towards to more and more smaller dimensions, hence the minimum channel length is shrinking continuously. In the MOSFET device, if the length of the channel  $L$  is reduced up to certain extent, then the speed of the device increases and hence, the device will perform faster. Simultaneously, the number of component per chip also increases. Due to reduction in the channel length of the device, the so called Short Channel Effects (SCE) arises. These effects are DIBL (Drain Induced Barrier Lowering), Punch Through, Hot Electron Reliability, Sub-threshold Current, Oxide Breakdown which severely affects MOS device performance [1].

In 1964, the SOI technology was developed to enhance the performance of conventional MOSFET.

These were partially and fully developed devices fabricated on Silicon on Sapphire (SOS) substrate which comes under substrate engineering. SOS technology was popularly used for various applications like in communication ICs, military and civilian applications and still is used in realization of HF circuits [2].

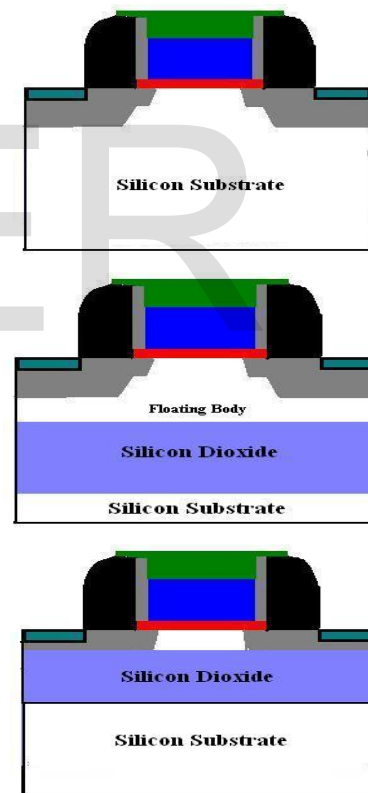


Figure 1: (a) Bulk MOSFET (b) Partially depleted SOI MOSFET (c) Fully depleted SOI MOSFET [3]

The Bulk MOSFET, Partially Depleted SOI MOSFET and Fully Depleted SOI MOSFET have shown in figure.1. In Partially Depleted SOI MOSFET, body is partially depleted and floats

independent from bulk substrate. In fully depleted MOSFET, substrate is replaced by Silicon dioxide ( $\text{SiO}_2$ ) and in these devices the gate is connected to the floating body. These devices have good HF characteristics, reduced body effect, improved current drive and ideal sub-threshold characteristics. In CMOS applications at sub-100nm, fully depleted SOI MOSFETs are very promising and attractive devices because of their low body effect coefficient and ideal sub-threshold slope. Microprocessors based on SOI technology have 22% improved speed over bulk CMOS [2].

Now moving from substrate engineering to gate engineering, there was more improvement in the device in the terms of area, power and speed of VLSI circuits, hence the concept of gate engineering have been introduced and special multiple-gate structure devices have been proposed [3]-[4]. Multiple-gate devices include the double-gate, triple-gate and FinFET structures. The requirement of small fin width or body thickness is relaxed by more advance devices like triple-gate, pi-gate, and omega-gate transistors. It is well known that the double-gate (top and bottom gate) silicon-on-insulator (SOI) MOSFET and the gate-all-around device are the most suitable device structures for reducing short-channel effects such as DIBL and sub threshold slope degradation [5]-[6]. One of the most important multi-gate structure is FinFET which shown better Sub-Threshold Swing and Drain-Induced Barrier Lowering and optimum ratio of gate length to Fin width [7]-[8]. The result shows that Multi-gate MOSFETs have shown better results in sub-threshold performances. In this paper, the performance evaluation of Double-Gate and FinFET structures have been discussed.

## II. DOUBLE GATE SOI MOSFET

After source/drain engineering and substrate engineering, the new approach has been evolved and known as gate engineering. In this paper, the new and the alternative transistor structure called the double-gate SOI MOSFET will be discussed and its efficiency in suppressing Short Channel Effects such as Drain-Induced Barrier Lowering (DIBL) and Hot-Carrier Effects, all of which affect the reliability of ultra-small geometry MOSFETs. The figure 2 and

figure 3 have shown the structure of double gate MOSFET and its circuit symbol. Here two gates control the channel potential. The DG-FET achieves better gate control and thereby has improved SCE. It does not suffer from electric field penetration from the source/drain to the channel through the buried oxide and is therefore more scalable [5]-[7].

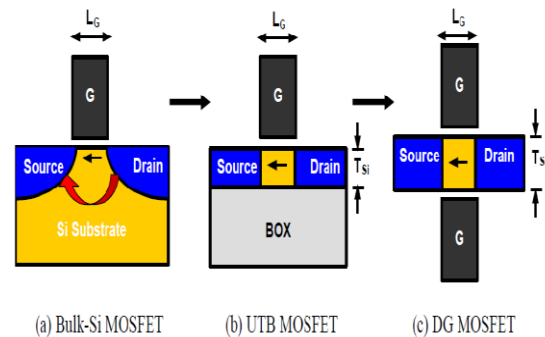


Figure 2: (a) Bulk MOSFET (b) UTB MOSFET and (c) DG MOSFET [5]

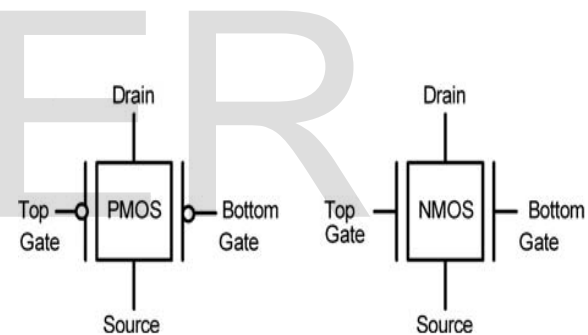


Figure 3: DG-MOSFET circuit symbols [6]

## III. FinFET

In this paper, we will discuss the FinFET structure. FinFETs are a variation of the typical DG configuration. This novel structure solves a series of scalability problems and also demonstrates suppressed SCEs than conventional MOSFET. FinFETs offer the advantages of easy fabrication process and lower source/drain resistance over typical double gate devices. A heavily doped poly-Si film forms the electrical contact of the device which wraps around the fin and the body of the MOSFET is served by the thin lightly doped Si in FinFET [9]-[10].

The dielectric spacer reduces the gap of the source/drains pads. At 17nm, the smallest gate length is achieved. Besides, this superior device is compatible to the planar CMOS fabrication platform and thereby considered economically efficient. FinFET is also demonstrated to be suitable for scaling. It is one of the most promising self-aligned structures that have so far been proposed. It consists of a thin Si fin with gate running over the fin in a self-aligned manner. Figure 4 and 5 show the FinFET structure [8].

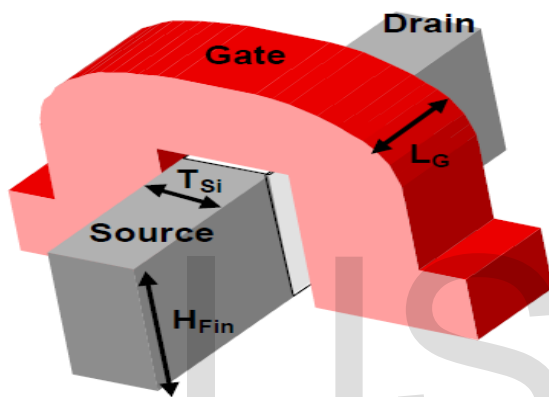


Figure 4: In FinFET the width of the channel is twice the height of the fin i.e.  $H_{FIN}$  [9]. Channel and sidewalls of the fin is controlled by gate.

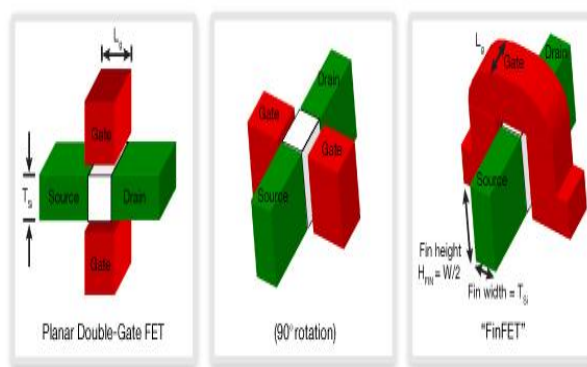


Figure 5: The FinFET Structure [10]

#### IV. SIMULATION RESULTS AND DISCUSSION

Using the Device Simulation Tool i.e. Atlas software package from Silvaco, the device electrical

properties were simulated. The gate oxide thickness and the buried oxide thickness is 3 nm and 100nm respectively. In this paper, double-gate (DG) MOSFET and FinFET device have been simulated using SILVACO TCAD tools and its various characteristics are plotted. For the good performance of the device, it is important for the back gate to control the threshold voltage ( $V_T$ ) of the front gate. This is helpful in optimization of different circuits in terms of delay, area and power. For Double-Gate MOSFET, process simulation with various materials have been studied and simulated by ATHENA Simulator as shown in figure 6. Next, by the help of ATLAS Simulator, the drain current vs drain voltage characteristics and drain current vs gate bias voltage have been simulated for above mentioned structure as shown in figure 7 and 8 respectively.

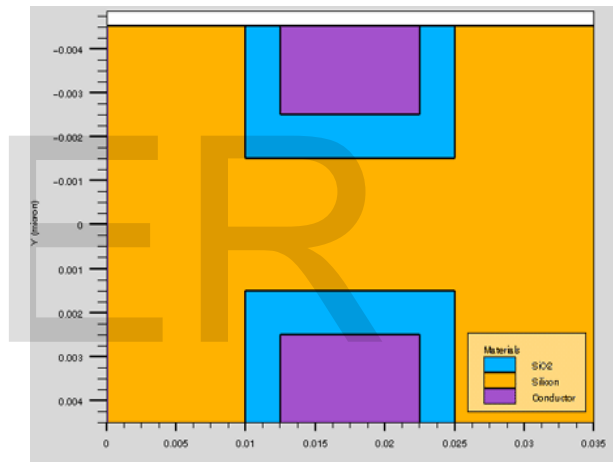


Figure 6: Process Simulation with Materials of Double Gate MOSFET

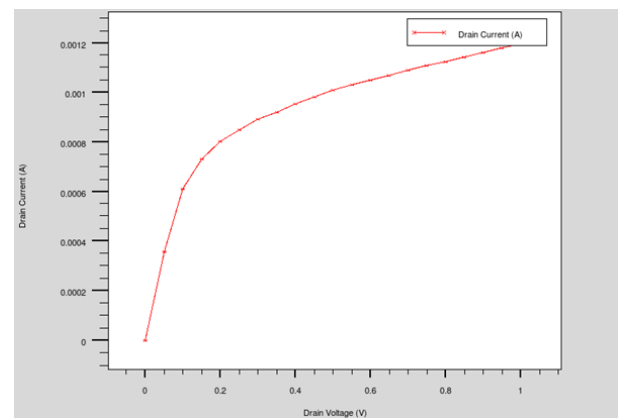
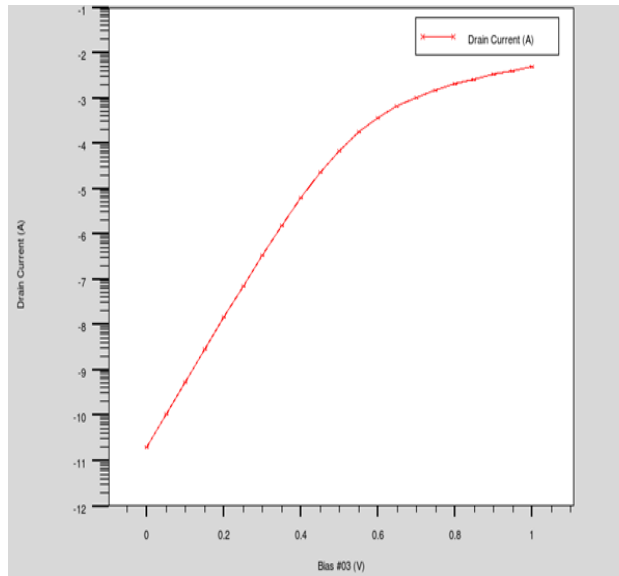
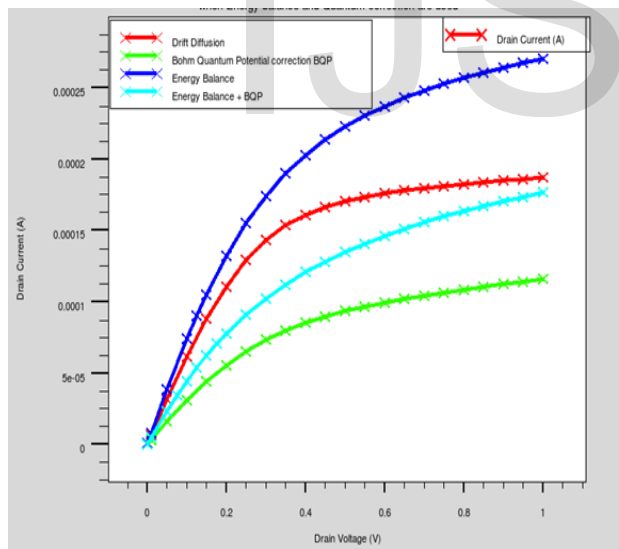


Figure 7: Drain Current Vs Drain Voltage Characteristics of Double Gate MOSFET



**Figure 8: Drain Current Vs Gate Bias Voltage Characteristics of Double Gate MOSFET**

In figure 9, the drain current vs drain voltage characteristics have been studied and simulated by the help of more advance version of 3D- SILVACO TCAD Tool.



**Figure 9: Drain Current Vs Drain Voltage Characteristics of FinFET**

## V. CONCLUSION

In this paper, we have analyzed and simulated the DG MOSFET and FinFET by the help of SILVACO TCAD Tool. We have also thoroughly examined the short channel effects like Sub-threshold effect, DIBL,

Breakdown phenomenon and their various parameters. The results show that DGMOSFET and FinFET have better results than conventional MOSFET. FinFET is the better option than DGMOSFET due less short channel effects.

## VI. FUTURE SCOPE

To seek possible alternatives for bulk MOSFETs beyond 30nm technology node, a number of novel multi-gate MOSFETs have been proposed in research, including Tri-Gate, Surrounding Gate [8], Pi Gate and Omega-Gate. Numerical simulation and analysis have shown better scalability of multi-gate MOSFETs over bulk MOSFETs. The better scalability allows multi-gate MOSFETs to scale down to shorter gate length with same off- current or produce less off-current with same gate length, thereby achieving better power- speed product.

## VII. ACKNOWLEDGEMENT

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